REMARKS

Claims 1-49 were originally filed in the present application. No claims were previously or are presently canceled or added. Thus, claims 1-49 remain pending in the present application.

Reconsideration of this application in light of the following remarks is requested.

Rejections under 35 U.S.C. §102(e)

Claims 1, 5, 8-12, and 44 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 20050093021, having Ouyang, et al., named as inventor ("Ouyang"). However, rejections based on 35 U.S.C. §102(e) cannot be supported by Ouyang as applied to claims 1, 5, 8-12, and 44 for at least the following reasons.

Claim 1

Claim 1 recites:

> 1. A semiconductor device, comprising:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and
> a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes one of:
> first source/drain regions recessed within the surface; and
> first source/drain regions extending from the surface; and
> wherein a second one of the NMOS and PMOS devices includes one of:
> second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;
> second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and
> second source/drain regions substantially coplanar with the surface.

The PTO provides in MPEP §2131 that "[t]o anticipate a claim, the reference must teach every element of the claim." Therefore, to support a rejection with respect to claim 1, Ouyang must contain all of the elements of claim 1. However, Ouyang does not disclose an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

In contrast, while Ouyang presents multiple alternate embodiments, each embodiment disclosed in Ouyang teaches source/drain regions of both NMOS and PMOS devices as being coplanar with the substrate surface. Applicants note that the Examiner cites paragraph [0040] of Ouyang as allegedly teaching a PMOS with recessed source/drain regions and an NMOS with source/drain regions that are coplanar to the substrate surface. However, Ouyang includes no such disclosure.

As shown in Figs. 2B, 3E, and 4B of Ouyang, the PMOS source/drain regions 10 and the NMOS source/drain regions 70 are always coplanar with one another – only the trench isolation 54 and the gate stack (dielectric 53, gate 52, and gate cover/spacers 51) are not coplanar with the substrate, because they extend above the substrate. For example, in Fig. 4B, which corresponds to paragraph [0040] cited by the Examiner, the source/drain regions 10 and 70 are coplanar with one another, such that it is impossible for either pair of source/drain regions (e.g., 10) to extend above the substrate, or to be recessed within the substrate, to a different degree than the other pair of source/drain regions (e.g., 70). Nonetheless, it requires close inspection of the left-hand side of Fig. 4B to discover that the source/drain regions 70 extend *through* layer 30, then layer 20, and finally extending into body 40'. Likewise, source/drain regions 10 also span layer 30, then

layer 20, and then extend into body 40 to the same depth as the source/drain regions 70 extend into body 40'.

Thus, it is clear that Ouyang fails to anticipate claim 1 and its dependent claims. Consequently, Applicants respectfully request the Examiner withdraw the §102 rejection of claims 1, 5, and 8-12.

Claim 44

Claim 44 recites:

> 44. A method of manufacturing a semiconductor device, comprising:
> forming an isolation region located in a substrate;
> forming an NMOS device located partially over a surface of the substrate; and
> forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes one of:
> first source/drain regions recessed within the surface; and
> first source/drain regions extending from the surface; and
> wherein a second one of the NMOS and PMOS devices includes one of:
> second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;
> second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and
> second source/drain regions substantially coplanar with the surface.

Ouyang also cannot support a §102 rejection of claim 44, because Ouyang fails to disclose forming an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending

from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface, as described above and as recited in claim 44.

Consequently, Applicants respectfully request the Examiner withdraw the §102 rejection of claim 44.

Rejections under 35 U.S.C. §103(a): Ouyang in view of Dawson

Claims 2-4, 13, 14, 16-18, 21-26, 28, 29, 32-36, 45, and 46 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ouyang in view of U.S. Patent No. 5,963,803 to Dawson, et al. ("Dawson"). Applicants traverse these rejections on the grounds that Ouyang and Dawson are defective in establishing a *prima facie* case of obviousness with respect to claims 1, 16, 28 and 44 and their respective dependent claims.

Claim 1

As the PTO recognizes in MPEP §2142:

> *The Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the Examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness.*

The Examiner cannot establish a *prima facie* case of obviousness based on the combination of Ouyang and Dawson in connection with claim 1 since 35 U.S.C. §103(a) provides that:

> *[a] patent may not be obtained ... if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains ... (emphasis added).*

Thus, when evaluating a claim for determining obviousness, all limitations of the claim must be evaluated. However, as described above, Ouyang fails to teach any of the configurations recited in claim 1. Moreover, Dawson fails to cure this shortcoming, because Dawson also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively. That is, Dawson fails to teach any of the configurations recited in claim 1 in the manner described above with respect to the deficiencies of Ouyang.

Therefore, it is impossible to render obvious the subject matter of claim 1 based on the combination of Ouyang and Dawson, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 1 or its dependent claims.

There is still another compelling, and mutually exclusive, reason why the combination of Ouyang and Dawson cannot be combined and applied to reject claim 1 under 35 U.S.C. §103(a).

The PTO also provides in MPEP §2142:

> *[T]he Examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the Examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. ...[I]mpermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.*

Here, the combination of Ouyang and Dawson does not teach, or even suggest, the desirability of combination since neither Ouyang nor Dawson teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively. That is, neither Ouyang nor Dawson teaches any of the configurations recited in claim 1 in the manner described above.

Thus, neither Ouyang nor Dawson provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Ouyang and Dawson to support a 35 U.S.C. §103(a) rejection of claim 1. Consequently, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1 and its dependent claims 2-4, 13, and 14.

Claim 16

Claim 16 recites:

> 16. A semiconductor device, comprising:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and
> a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes:
> first source/drain regions located at least partially in the substrate; and
> a first gate interposing the first source/drain regions and having a first gate height over the surface; and
> wherein a second one of the NMOS and PMOS devices includes:
> second source/drain regions located at least partially in the substrate; and
> a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Ouyang and Dawson, whether alone or in combination, do not teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region located in the substrate between the NMOS and PMOS devices, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial

difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

That is, as described above, Ouyang fails to provide such disclosure. Moreover, Dawson fails to cure this shortcoming. In contrast, as shown in Figs. 1G-1L of Dawson, Dawson only teaches source/drain regions 130/132/140/142/150/152/160/162 which are each coplanar with the substrate.

Therefore, it is impossible to render obvious the subject matter of claim 16 based on the combination of Ouyang and Dawson, and the above explicit terms of §103 cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 16 and its dependent claims.

There is still another compelling, and mutually exclusive, reason why the combination of Ouyang and Dawson cannot be applied to reject claim 16 under 35 U.S.C. §103(a). Here, the combination of Ouyang and Dawson does not teach, or even suggest, the desirability of combination since neither teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, neither Ouyang nor Dawson provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Ouyang and Dawson to support a 35 U.S.C. §103(a) rejection of claim 16. Consequently, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of

obviousness cannot be met with respect to claim 16, and the rejection under 35 U.S.C. §103(a) is not applicable to claim 16 or its dependent claims.

Claim 28

Claim 28 recites:

> 28. A semiconductor device, comprising:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and
> a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes:
> first source/drain regions located at least partially in the substrate;
> a first gate interposing the first source/drain regions; and
> first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and
> wherein a second one of the NMOS and PMOS devices includes:
> second source/drain regions located at least partially in the substrate;
> a second gate interposing the second source/drain regions; and
> second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Ouyang and Dawson, whether alone or together, also do not teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and

wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively, as recited in claim 28.

Therefore, it is impossible to render obvious the subject matter of claim 28 based on Ouyang and Dawson, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28, and a rejection under 35 U.S.C. §103(a) is not applicable.

Moreover, Ouyang and Dawson fail to provide any incentive or motivation for the modification suggested by the Examiner to arrive at the recitation of claim 28. Therefore, there is simply no basis in the art of record for combining Ouyang and Dawson as suggested by the Examiner to support a 35 U.S.C. §103(a) rejection of claim 28 and its dependent claims. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28 and its dependent claims.

Claim 44

As described above, Ouyang and Dawson each fail to teach any of the configurations recited in claim 44. Therefore, it is impossible to render obvious the subject matter of claim 44 based on the combination of Ouyang and Dawson, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 44, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 44 and its dependent claims.

There is still another compelling, and mutually exclusive, reason why the combination of Ouyang and Dawson cannot be applied to reject claim 44 under 35 U.S.C. §103(a). Here, the combination of Ouyang and Dawson does not teach, or even suggest, the desirability of

combination since neither teach or suggest forming an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

Thus, neither Ouyang nor Dawson provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Ouyang and Dawson to support a 35 U.S.C. §103(a) rejection of claim 44. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 44 and its dependent claims.

Rejections under 35 U.S.C. §103(a): Ouyang in view of Yeo

Claims 38, 39, and 42 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ouyang in view of U.S. Patent Application Publication No. 20040173815, having Yeo, et al., named as inventor ("Yeo"). Applicants traverse these rejections on the grounds that Ouyang and Yeo are defective in establishing a *prima facie* case of obviousness with respect to independent claim 38 and its dependent claims.

Claim 38

Claim 38 recites:

> 38. A semiconductor device, comprising:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and
> a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes one of:

first source/drain regions located at least partially within the substrate and comprising SiC; and
first source/drain regions located at least partially within the substrate and comprising SiGe; and
wherein a second one of the NMOS and PMOS devices includes one of:
second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe;
second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and
second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

As described above and in previous responses to office actions, Ouyang and Yeo, whether alone or together, fail to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Thus, for at least this reason, the combination of Ouyang and Yeo fails to support a *prima facie* case of obviousness of claim 38 and its dependent claims.

Another compelling and mutually exclusive reason why the combination of Ouyang and Yeo cannot be combined and applied to reject claim 38 under 35 U.S.C. §103(a) is that the combination of Ouyang and Yeo does not teach, or even suggest, the desirability of combination since neither teach or suggest an NMOS device and a PMOS device each located partially over a

substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Thus, neither Ouyang nor Yeo provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Ouyang and Yeo to support a 35 U.S.C. §103(a) rejection of claim 38. Accordingly, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 38 and its dependent claims.

Rejections under 35 U.S.C. §103(a): Ouyang in view of Okumura

Claim 47 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ouyang in view of U.S. Patent No. 5,428,239 to Okumura, et al. ("Okumura"). Applicants traverse these rejections on the grounds that the combination of Ouyang and Okumura is defective in establishing a *prima facie* case of obviousness with respect to independent claim 47.

Claim 47

Claim 47 recites:

> 47. An integrated circuit device, comprising:
> a plurality of semiconductor devices each including:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
wherein, in ones of the plurality of semiconductor devices, a first one of the NMOS and PMOS devices includes one of:
first source/drain regions recessed within the surface; and
first source/drain regions extending from the surface; and
wherein, in ones of the plurality of semiconductor devices, a second one of the NMOS and PMOS devices includes one of:
second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;
second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and
second source/drain regions substantially coplanar with the surface; and
a plurality of interconnects connecting ones of the plurality of semiconductor devices.

To support a rejection with respect to claim 47, the combination of Ouyang and Okumura must contain all of the elements of claim 47. However, the combination of Ouyang and Okumura fails to teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region in the substrate, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

There is still another compelling, and mutually exclusive, reason why the combination of Ouyang and Okumura cannot be combined and applied to reject claim 47 under 35 U.S.C. §103(a). That is, the combination of Ouyang and Okumura does not teach, or even suggest, the desirability of combination since neither Ouyang nor Okumura teach or suggest an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region in the substrate, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

Thus, neither Ouyang nor Okumura provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Ouyang and Okumura to support a 35 U.S.C. §103(a) rejection of claim 47. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 47.

Rejections under 35 U.S.C. §103(a): Ouyang in view of Dawson and Shimizu

Claims 27 and 37 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ouyang in view of Dawson and Shimizu. Applicants traverse these rejections on the grounds that this combination is defective in establishing a *prima facie* case of obviousness with respect to their respective independent claims 16 and 28.

Claim 16

Ouyang, Dawson, and Shimizu, whether alone or in combination, do not teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region located in the substrate between the NMOS and PMOS devices, wherein a first

one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

That is, as described above, Ouyang and Dawson each fail to provide such disclosure. Moreover, Shimizu fails to cure this shortcoming, as described in previous responses to office actions.

Therefore, it is impossible to render obvious the subject matter of claim 16 based on the combination of Ouyang, Dawson, and Shimizu, and the above explicit terms of §103 cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 16 and its dependent claims.

There is still another compelling, and mutually exclusive, reason why the combination of Ouyang, Dawson, and Shimizu cannot be applied to reject claim 16 under 35 U.S.C. §103(a). Here, the combination of Ouyang, Dawson, and Shimizu does not teach, or even suggest, the desirability of combination since none of these references teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial

difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, neither Ouyang, Dawson, nor Shimizu provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Ouyang, Dawson, and Shimizu to support a 35 U.S.C. §103(a) rejection of claim 16. Consequently, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16, and the rejection under 35 U.S.C. §103(a) is not applicable to claim 16 or its dependent claims.

Claim 28

Ouyang, Dawson, and Shimizu, whether alone or together, also do not teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively, as recited in claim 28.

Therefore, it is impossible to render obvious the subject matter of claim 28 based on Ouyang, Dawson, and Shimizu, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28 or its dependent claims, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 28 or its dependent claims.

Moreover, Ouyang, Dawson, and Shimizu fail to provide any incentive or motivation for the modification suggested by the Examiner to arrive at the recitation of claim 28. Therefore, there is simply no basis in the art of record for combining Ouyang, Dawson, and Shimizu as suggested by the Examiner to support a 35 U.S.C. §103(a) rejection of claim 28 and its dependent claims. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28 and its dependent claims.

Rejection under 35 U.S.C. §103(a): Ouyang in view of Yeo and Shimizu

Claim 43 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ouyang in view of Yeo and Shimizu. Applicants traverse this rejections on the grounds that this combination is defective in establishing a *prima facie* case of obviousness with respect to independent claim 38.

Claim 38

As described above and in previous responses to office actions, Ouyang and Yeo, whether alone or together, fail to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe. Moreover, as also described in previous response to office actions, Shimizu also fails to provide such disclosure.

Thus, for at least this reason, the combination of Ouyang, Yeo and Shimizu fails to support a *prima facie* case of obviousness of claim 38 and its dependent claims.

Another compelling and mutually exclusive reason why the combination of Ouyang, Yeo and Shimizu cannot be combined and applied to reject claim 38 under 35 U.S.C. §103(a) is that the combination of Ouyang, Yeo and Shimizu does not teach, or even suggest, the desirability of combination since none of the references teach or suggest an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Thus, neither Ouyang, Yeo nor Shimizu provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Ouyang, Yeo and Shimizu to support a 35 U.S.C. §103(a) rejection of claim 38. Accordingly, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 38 and its dependent claims.

Conclusion

It is clear from the foregoing that independent claims 1, 16, 28, 38, 44 and 47 are in condition for allowance. Dependent claims 2-15, 17-27, 29-37, 39-43, 45, 46, 48 and 49 depend from and further limit independent claims 1, 16, 28, 38, 44 and 47, in a patentable sense. Therefore, claims 2-15, 17-27, 29-37, 39-43, 45, 46, 48 and 49 are also in condition for allowance.

Consequently, an early formal notice of allowance of claims 1-49 is requested.

Respectfully submitted,

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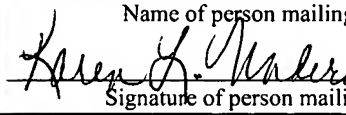

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